# <<Verilog HDL高级数字设计>>

## 图书基本信息

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## 前言

Simplify,Clarify, and Verify Behavioral modeling with a hardware description language （HDL） is the key to modern design of application-specific integrated circuits （ASICs）. Today, most designers use an HDL-based design method to create a high-level, language-based, abstract description of a circuit, and verify its functionality and timing. The language used to teach design methodology in the first edition of this text, IEEE 1464-1995, has undergone two revisions to improve the effectiveness and efficiency of the language: IEEE 1364-2001 followed by a revision in 2005, known as Verilog-2001 and Verilog-2005, respectively. The motivation behind this edition is basically the same as that which guided the first edition: students preparing to contribute to a productive design team must know how to use a HDL at key stages of the design flow. Thus, there is a need for a course going beyond the basic principles and methods learned in a first course in digital design. This book is written for such a course. The quantity of books discussing HDLs far exceeds that which was available at the time of the first edition, and most of these are still oriented toward explanations of language syntax, rather than toward design, and are not well-suited for classroom use. Our focus is on design methodology enabled by an HDL. Thus, the language itself has a subordinate role. In this edition, we have made a strong effort to demonstrate by examples the importance of partitioning a digital machine to expose its datapath, status （feedback） signals, and controller （finite state machine）.This effort leads, we think, to a much clearer and straightforward approach to designing and verifying complex digital machines. We present an abundance of simulation results, with annotation to help students （1） understand the operation of a sequential machine and （2） appreciate the time-sequential interaction between the signals produced by the controller, the operations in the datapath, and the signals reported back to the controller from the datapath, all with the aim of developing synthesizable, latch-free, race-free designs.

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## 内容概要

本书依据数字集成电路系统工程开发的要求与特点，利用Verilog HDL对数字系统进行建模、设计与验证，对ASIC/FPGA系统芯片工程设计开发的关键技术与流程进行了深入讲解，内容包括：集成电路芯片系统的建模、电路结构权衡、流水、多核微处理器、功能验证、时序分析、测试平台、故障模拟、可测性设计、逻辑综合、后综合验证等集成电路系统的前后端工程设计与实现中的关键技术及设计案例。
书中以大量设计实例叙述了集成电路系统工程开发需遵循的原则、基本方法、实用技术、设计经验与技巧。
本书既可作为电子与通信、电子科学与技术、自动控制、计算机等专业领域的高年级本科生和研究生的教材或参考资格，也可用于电子系统设计及数字集成电路设计工程师的专业技术培训。

## 作者简介

Michael D.Ciletti，科罗拉多大学电气与计算机工程系教授。
研究方向包括通过硬件描述语言进行数字系统的建模、综合与验证、系统级设计语言和FPGA嵌入式系统。
其著作还有Digital Design，Fourth Edition(其翻译版和影印版均由电子工业出版社出版)。
作者曾在惠普、福特微电子和

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## 书籍目录

## 章节摘录

HDL-based designs are easier to debug than schematics.A behavioral descrip-tion encapsulating complex functionality hides underlying gate-level detail，so there isless information to cope with in trying to isolate problems in the functionality of thedesign.Furthermore.if the behavioral description is functionally correct.it is a goldstandard for subsequent gate.1evel realizations. HDL-based designs incorporate documentation within the design by using de-scriptive names，by including comments to clarify intent，and by explicitly specifying ar-chitectural relationships.thereby reducing the volume of documentation that must bekept in other archives.Simulation of a language.based model explicitly specifies thefunctionality of the design.Since the language is a standard.documentation of a designcan be decoupled from a particular vendors tools. Behavioral modeling is the predominant descriptive style used by industry，en-abling the design of massive chips.Behavioral modeling describes the functionality Dr adesign by specifying what the designed circuit will do.not how to build it in hardware.It specifies the input-output model of a logic circuit and suppresses details about phys-ical，gate-level implementation. Behavioral modeling encourages designers to（1）rapidly create a behavioral pro-totype of a design（without binding it to hardware details），（2）verify its functionality,and then （3） use a synthesis tool to optimize and map the design into a selected physi-cal technology.If the model has been written in a synthesis-ready style，the synthesistool will remove redundant logic.perform tradeoffs between alternative architecturesand／or multilevel equivalent circuits.and ultimately achieve a design that is compatiblewith area or timing constraints.By focusing the designers attention on the functional-ity that is to be implemented rather than on individual logic gates and their intercon-nections.behavioral modeling provides the freedom to explore alternatives to a designbefore committing it to production. Aside from its importance in synthesis.behavioral modeling provides flexibilityto a design project by allowing parts of the design to be modeled at difierent levels of abstraction.The Verilog language accommodates mixed levels of abstraction so thatportions of the design that are implemented at the gate level（i-e structurally）can beintegrated and simulated concurrently with other parts of the design that are repre-sented by behavioral descriptions. 1.1.4 Simulation and Functional VerificationThe functionality of a design is verified（Step 4 in Figure 1-1） either by simulation or byformaI methods［7］.Our discussion will focus on simulation that is reasonable for the size of circuits we can present here.The design flow iterates back to Step 3 untiI thefunctionality of the design has been verified.The verification process is threefold ；itincludes（1）development of a test plan，（2）development of a testbench，and（3）execu-tion of the test.

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## 编辑推荐

《Verilog HDL高级数字设计（第2版）（英文版）》特色 ·重点讨论现代数字电路系统的设计方法 ·阐述并推广基于Verilog 2001和2005，且可综合的RTL描述和算法建模的设计风格 ·明确指出了可综合和不可综合循环的区别 ·讲述了如何应用ASM和ASMD图进行行为级建模 ·深入讨论基于Verilog 2001和2005的数字处理系统、RISC计算机和各种数据通道控制器、异步和同步FIFO设计的算法和架构及综合的设计实例 ·给出了150多个经过完全验证的实例，对时序分析、故障模拟、测试和可测性设计进行切合实际的讨论 ·含有利用Vetilog 2001和2005编写的具备JTAG和BIST可测功能的实用设计案例 ·每章后均设计了一些涉及面广且难度高的习题 ·包含一套与《Verilog HDL高级数字设计（第2版）（英文版）》内容配套的可适合实验室实验验证的FPGA设计实例，如ALU、可编程电子锁、有FPFO的键盘扫描器、可纠错的串行通信接口、基于SRAM的控制器、异步和同步FIFO设计、存储器及RISC CPU 《Verilog HDL高级数字设计（第2版）（英文版）》支持网站内容包括：所有模型的源文件、仿真实例的测试平台源文件、幻灯片文件、某些工具软件的速 成教案及常见问题解答（FAQ）

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